VirtuosoNext Performance

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Revision history

Antonio Ramos	Creation	30.03.2015
Bernhard Sputh	Updated the ARM-Cortex-M3 and A9 Codesizes	07.09.2015
Bernhard Sputh	Adding Loop figures for the TI-C6000	06.07.2016
Bernhard Sputh	Adding Latency figures for the TI-C6000	18.07.2016

1. Introduction

These benchmarks try to provide realistic figures by using real-world target boards. The per will differe from board to board even when using the same processor chips because the board designs are different, e.g. the memory might be slower or share the bus with other devices, therefore introducing wait states.

The dependency on the compiler is taken into account by compiling with different compiler switches. Code sizes include the runtime overhead imposed by the compiler as well.

2. ARM-Cortex-A9 on OMAP4460

Phytec board properties:

- 512 MB of DDR-RAM
- 56 KB of SRAM
- 32 KB instruction cache and 32 KB data caches per CPU (Level 1)
- 700MHz Core Clock
- Communication link: RS232 at 115200 bps

2.1 Code Size

The given code sizes are measured by compiling different examples with Compile-Option `Os' and Debug-Option `0' in OCR 1.6, see Table 1. PI stands for Priority Inheritance.

	PI Enabled		PI Disabled	
	Elf .text segment	Mapfile Analysis	Elf .text segment	Mapfile Analysis
Kernel	15004			
+Task	15004			
+ Port	15252			
+ Event	15364			
+ Semaphore	15596			
+ Resource	15852			
+ BlackBoard	16972			
+ DataEvent	17676			
+ FIFO	18564			
+ MBQ	21844			

Table 1: Code sizes for ARM-Cortex-A on OMAP44660, including the BSP (Board Support Package).

2.2 Semaphore Loop Time

Figures obtained using an ARM-Cortex-A9 core at 700MHz with VirtuosoNext-1.0 and the OMAP4460.

Compile-switch:

- O0: 14.89 usec per loop (.text = 29196 byte)
- O3: 11.59 usec per loop (.text = 16980 byte)
- Os: 11.88 usec per loop (.text = 15676 byte)

2.3 Semaphore Loop Time SMP

Figures obtained using a SemaphoreLoop distributed over core 1 and core 2 of the ARM-Cortex-A9 at 700MHz with VirtuosoNext-1.0 and the OMAP4 BSP, and the Shared Memory Link Driver. The code is placed in DDR RAM, the shared memory in the internal SRAM:

- O0: 37.85 usec per loop (core0 .text = 40492 byte, core1 .text = 39372 byte)
- O3: 30.13 usec per loop (core0 .text = 23412 byte, core1 .text = 22564 byte)
- Os: 30.47 usec per loop (core0 .text = 20468 byte, core1 .text = 19636 byte)

2.4 Interrupt Latency

Figures obtained using an ARM-Cortex-A9 core at 700MHz with OCR 1.6 on the OMAP4460. The link between the ARM-Cortex-A9-Node and the Win32-Node was established using a RS232 link.

Compile-switch:

- O0: .text = 53528 bytes,
  - IRQ → ISR: 202 – 1540 ns (50% at 376 ns)
  - IRQ → Task: 2704 – 6046 ns (50% at 4296 ns)
- O3: .text = 28600 bytes
  - IRQ → ISR: 138 – 1150 ns (50% at 420 ns)
  - IRQ → Task: 1726 – 4228 ns (50% at 2766 ns)
- Os: .text = 25624 bytes
  - IRQ → ISR: 156 – 1170 ns (50% at 434 ns)
  - IRQ → Task: 1824 – 4464 ns (50% at 3002 ns)

3. ARM-Cortex-M3 on LM3S6965 Eval Board

Board Specification:

- 64 KB of SRAM
- 50MHz CPU clock.
- Communication link: Ethernet Link using uIP.

3.1 Code Size

The given code sizes are measured by compiling different projects with Compile-Option `Os' and Debug-Option `0' in OCR 1.6, see Table 2.

	Elf .text segment in bytes	Elf .text segment in bytes (unpadded)
Kernel	16384	8376
+ Task	16384	8380
+ Port	16384	8560
+ Event	16384	8656
+ Semaphore	16384	8844
+ Resource	16384	9012
+ BlackBoard	16384	9740
+ DataEvent	16384	10220
+ FIFO	16384	10588
+ MBQ	16384	12668

Table 2: Code sizes for ARM-Cortex-M3 on LM3S6965 Eval Board, including the BSP

3.2 Semaphore Loop Time

Figures obtained using an ARM-Cortex-M3 core at 50MHz with OCR 1.6 for the LM3S6965.

Compile-switch:

- O0: 122.3 usec per loop (.text = 32768 byte padded, padding: 15572 byte, real code: 17196 byte)
- O3: 58.9 usec per loop (.text = 16384 byte padded, padding: 6908 byte, real code: 9476 byte)
- Os: 61.3 usec per loop (.text = 16384 byte padded, padding: 7724 byte, real code: 8660 byte)

3.3 Interrupt Latency

Figures obtained using an ARM-Cortex-M3 core at 50MHz with OCR-1.6 for the LM3S6965. The link between the ARM-Cortex-M3-Node and the Win32-Node was established using a TCPIP-LinkDriver.

Compile-switch:

- O0: .text = 65536 bytes padded, padding: 10488 byte, real code: 55048 byte
  - IRQ → ISR: 920 – 8980 ns (50% at 1000 ns)
  - IRQ → Task: 36 – 92 us (50% at 49 us)

- O3: .text = 65536 bytes padded, padding: 30412 byte, real code: 35124 byte
  - IRQ → ISR: 820 – 5020 ns (50% at 1020 ns)
  - IRQ → Task: 16 – 39 us (50% at 22 us)
- Os: .text = 32768 bytes padded, padding: 5980 byte, real code: 26788 byte
  - IRQ → ISR: 780 – 5180 ns (50% at 860 ns)
  - IRQ → Task: 17 – 41 us (50% at 21 us)

4. TI-C6000 for C6678 SoC

Board Specification:

- Platform: TI-C6000 (Parsec/Sundance VF360)
- Memory Protection: Not enabled.
- Code running in L2SRAM on Core0
- 1250MHz CPU clock.
- Communication link: UART.

4.1 Code Size

The given code sizes are measured by compiling different projects with Compile-Option `Os' and Debug-Option `0' in VirtuosoNext-1.1, see Table 3.

	Elf .text segment in bytes
Kernel	20692
+ Task	20724
+ Port	20956
+ Event	21116
+ Semaphore	21380
+ Resource	21608
+ BlackBoard	22848
+ DataEvent	23536
+ FIFO	24284
+ MBQ	26448

Table 3: Code sizes for TI-C6000 SoC TI-C6678 on, Parsec VF360 including the BSP

4.2 Semaphore Loop Time

Figures obtained using Core0 of a C6678 in the Parsec VF360 at 1250MHz with VirtuosoNext 1.1.

Compile-switch:

- O0: 6.55 usec per loop (.text = 30020 byte)
- O3: 2.81 usec per loop (.text = 25980 byte)
- Os: 4.75 usec per loop (.text = 21160 byte)

4.3 Interrupt Latency

Figures obtained using Core0 of a C6678 in the Parsec VF360 at 1250MHz with VirtuosoNext 1.1.. The link between the C6678-Node and the Win32-Node was established using an UART-LinkDriver running with 115200bps. The L1 cache was enabled with 32kB data cache and 32kB instruction cache. The interrupt was passed directly through INTB, avoiding the otherwise necessary interrupt dispatching in software.

Compile-switch:

- O0: .text = 51908 bytes
  - IRQ → ISR: 176 – 388 ns (50% at 176 ns)

    - IRQ → Task: 1812 – 3728 ns (50% at 2152 ns)
- O3: .text = 45040 bytes
    - IRQ → ISR: 160 – 260 ns (50% at 176 ns)
    - IRQ → Task: 936 – 1728 ns (50% at 1188 ns)
- Os: .text = 35680 bytes
    - IRQ → ISR: 172 – 316 ns (50% at 172 ns)
    - IRQ → Task: 1460 – 2768 ns (50% at 1788 ns)